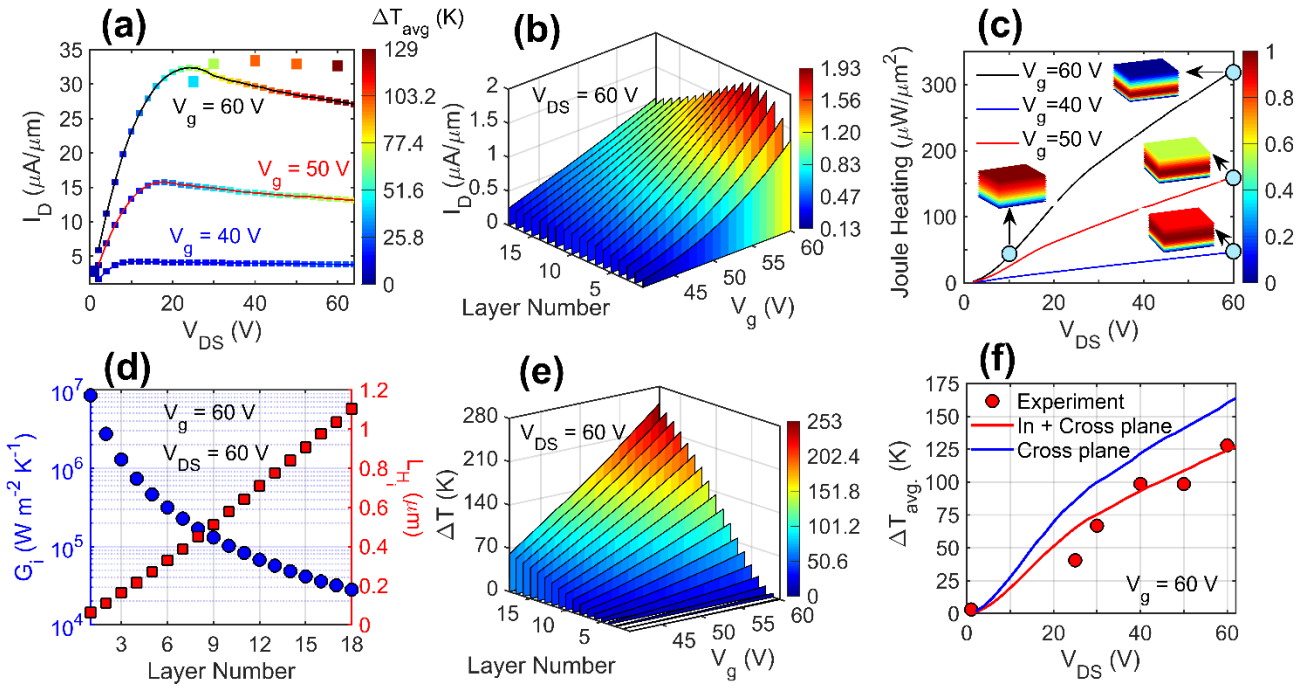
Power Dissipation and Self-Heating in Few-Layered (FL) 2D Materials



(a) I_D–V_{DS} output characteristics in 18-layer WSe_2 with different V_g calculated at room temperature (300 K). The color of square markers represents the rise in average device temperature ΔT_{avg} at each V_{DS} and V_g. Large square colored markers denote experimentally measured I_D, and ΔT_{avg} with V_{DS} at V_g equals 60 V. (b) Drain current per layer for different gate voltages V_g at V_{DS} = 60 V. (c) Joule heating versus V_{DS} at different V_g. The insets show Joule heating among layers at different V_{DS} and V_g. (d) Thermal boundary conductance G_i (left y-axis) and thermal healing length L_H (right y-axis) of each layer in an 18-layer WSe_2 stack. (e) Temperature rise in each layer for different V_g at V_{DS} equal to 60 V. (f) Calculated (red curve) and measured (red circles) average temperature rises of the stack versus V_{DS} at V_g equal 60 V. The blue curve represents the average temperature rise if the heat removal was entirely cross-plane.

Owing to their ultrathin nature and absence of dangling bonds, TMDCs like tungsten di-selenide (WSe_2) show a great promise to be used as channel material in future nanoelectronic transistors. While monolayer TMDCs suffer from low mobility due to substrate impurities, mobility is found to improve by one to two orders of magnitude in their FL counterparts. Understanding heat dissipation from hotspots in such devices is critical to their development and implementation as next-generation electronic devices. To quantify the impact of self-heating, I developed a coupled electro-thermal model where the distribution of current and resultant heat dissipation among layers are calculated at first [J9]. Then by using a FL-thermal boundary conductance (TBC) model based on phonon dispersion calculated from first principles [J4,J6], which I co-developed with one of my lab members, layer-resolved temperature-rise and steady-state current are solved self-consistently. We found an unexpected current re-routing mechanism which prevents severe degradation of mobility and hence reduces the impact of self-heating. We showed that both mobility and TBC depend on number of layers, and hence there exists an optimal number of layers for best device performance. Our model predicted that heterostructure stacks with both strong electrostatic screening and substrate/interlayer coupling would be the most desirable candidates for transistor applications.